CLAIMS:

1. A circuit, comprising:

a first logic circuit to operate in a first clock domain, said first logic circuit to generate a control signal;

a second logic circuit to operate in a second clock domain, said second logic circuit to receive said control signal; and

a synchronization circuit to synchronize said control signal between said first clock domain and said second clock domain using a time slot determined prior to receiving said control signal at said synchronization circuit.

2. The circuit of claim 1, wherein said first and second logic circuits are synchronous sequential logic circuits.

3. The circuit of claim 1, wherein said control signal is an asynchronous control signal between said first logic circuit and said second logic circuit.

4. The circuit of claim 1, wherein said first clock domain uses a first clock signal operating a first frequency, and said second clock domain uses a second clock signal operating at a second frequency.

5. The circuit of claim 4, wherein said first frequency is higher than said second frequency.

6. The circuit of claim 4, wherein said synchronization circuit synchronizes said control signal from said first clock signal to said second clock signal in zero to one clock cycle of said second clock signal.

7. The circuit of claim 4, wherein said synchronization circuit comprises:

a ratio circuit to receive said first clock signal and said second clock signal, said ratio circuit to synchronize said first clock signal and said second clock signal in accordance with a synchronization delay value, generate a clock ratio value to represent a clock ratio between said first clock signal and said second clock signal, and generate a rising edge indicator to indicate a rising edge for said second clock signal;

a window circuit to receive said first clock signal, said second clock signal, said clock ratio value and said rising edge indicator, said window circuit to determine said time slot, and generate a latch ready signal to represent a start time for said time slot; and

a latch to receive said latch ready signal, said first clock signal, and said control signal, said latch to synchronize said control signal to said second clock signal during said time slot indicated by said latch ready signal, and generate a synchronized control signal.

8. The circuit of claim 7, wherein said latch comprises a D flip-flop.

9. The circuit of claim 7, wherein said latch ready signal is asserted to indicate a start time for said time slot, and remains asserted for a time interval of at least one cycle of said first clock signal.

10. The circuit of claim 9, wherein said start time comprises at least one clock cycle of said first clock signal prior to a set up time for said second logic circuit clocked by said second clock signal.

11. The circuit of claim 1, wherein said first logic circuit comprises a source register to store data, and said second logic circuit comprises a destination register to receive said stored data, and said source registers sends said stored data to said destination register once said control signal has been synchronized.

12. A method, comprising:

generating a control signal from a first logic circuit operating in a first clock domain;

sending said control signal to a second logic circuit operating in a second clock domain; and

synchronizing said control signal from said first clock domain to said second clock domain using a predetermined time slot.

13. The method of claim 12, wherein said first clock domain uses a first clock signal operating at a first frequency, and said second clock domain uses a second clock signal operating at a second frequency.

14. The method of claim 13, wherein said first frequency is higher than said second frequency.

15. The method of claim 14, wherein said synchronization comprises:

receiving said first and second clock signals at a synchronization circuit;

synchronizing said first and second clock signals in accordance with a synchronization delay value;

determining a clock ratio value between said first and second clock signals;

generating a rising edge indicator for said second clock signal; and

determining said time slot using first and second clock signals, said clock ratio value, said rising edge indicator and said synchronization delay value.

16. The method of claim 15, further comprising generating a latch ready signal during said time slot.

17. The method of claim 16, wherein said latch ready signal is asserted to indicate a start time for said time slot, and remains asserted for a time interval of at least one cycle of said first clock signal.

18. The method of claim 17, wherein said start time comprises at least one clock cycle of said first clock signal prior to a set up time for said second logic circuit clocked by said second clock signal.

19. The method of claim 12, further comprising transferring said information from said first logic circuit to said second logic circuit once said control signal has been synchronized.

20. A system, comprising:

a communication medium;

a network node connected to said communication medium; and

wherein said network node comprises a plurality of logic circuits, with a first logic circuit to operate in a first clock domain and generate a control signal, a second logic circuit to operate in a second clock domain and receive said control signal, and a synchronization circuit to synchronize said control signal between said first clock domain and said second clock domain using a time slot determined prior to receiving said control signal at said synchronization circuit.

21. The system of claim 20, wherein said first clock domain uses a first clock signal operating a first frequency, said second clock domain uses a second clock signal operating at a second frequency, and said first frequency is higher than said second frequency.

22. The system of claim 21, wherein said synchronization circuit comprises:

a ratio circuit to receive said first clock signal and said second clock signal, said ratio circuit to synchronize said first clock signal and said second clock signal in accordance with a synchronization delay value, generate a clock ratio value to represent a clock ratio between said first clock signal and said second clock signal, and generate a rising edge indicator to indicate a rising edge for said second clock signal;

a window circuit to receive said first clock signal, said second clock signal, said clock ratio value and said rising edge indicator, said window circuit to determine said time slot, and generate a latch ready signal to represent a start time for said time slot; and

a latch to receive said latch ready signal, said first clock signal, and said control signal, said latch to synchronize said control signal to said second clock signal during said time slot indicated by said latch ready signal, and generate a synchronized control signal.